Intel Releases New PCIe Connector Metrology Collateral in Support of PCIe GEN3

Intel is committed to clear, accurate and accessible connector metrology that meets the needs of the PCIe GEN3 interconnect. Intel has upgraded its PCIe connector measurement reference design and procedures to extend the accuracy of measurement to the higher frequencies required of GEN3 PCIe connectors. In addition, new emphasis on how to take measurements has been added in an effort to improve repeatability.

Intel is releasing two items to support the new PCIe GEN3 connector performance requirements:

PCIe Gen 3 Connector High Speed Connector Evaluation Board (CEB) Reference Design*
PCIe Gen 3 Connector High Speed Electrical Test Procedure*

This reference design and the associated test procedure update and replace the previously released PCIe connector evaluation board to accurately measure PCIe connector performance to GEN3 limits.

The current connector evaluation board (CEB) designs are for measuring performance of GEN1 and GEN2 PCIe connectors. The GEN1 and GEN2 board designs contain many permutations of via/pad/anti-pad and add-in card pad sizes. The GEN1 and GEN2 board calibration structures are designed to provide accurate measurements to approximately 3 x Nyquist, 3.75 GHz and 7.5 GHz for GEN1 and GEN2 boards respectively.

The new GEN3 board is designed to evaluate PCIe connectors to GEN3 performance limits. The GEN3 board contains a single x4 PCIe footprint with standard via/pad/anti-pad and add-in card pad sizes. The calibration structures on the GEN3 board are designed to provide accurate measurements to 3 x GEN3 Nyquist frequencies (12 GHz). A comparison of the new features to the previous release is shown below in Table 1.

Table 1: *Comparison of PCIe Connector Metrology Characteristics and Features*

Existing PCIe Connector Metrology	New PCIe Connector Metrology
GEN1, GEN2 PCIe connector evaluation board, multiple-sites/multiple-add-in cards	GEN3 PCIe connector evaluation board, single-site/single-add-in card
Polyclad 370 PCB	Nelco 4000-SI/Nelco 4000-13 SI
Measure to 4 GHz	Measure to 20 GHz
SOLT, TRL Calibration	TRL Calibration
	CEB, CEB BOM, Support Bracket
	Characterization board design rules

GEN3 Measurement Collateral

The complete GEN3 collateral consists of the measurement procedure and the CEB design files. The measurement procedure (*PCIe* Gen 3 Connector High Speed Electrical Test Procedure*) includes the CEB bill of materials, and a measurement template. The board design file (*PCIe* Gen 3 Connector High Speed Connector Evaluation Board (CEB) Reference Design*) includes all Cadence Allegro* board design files, fab drawing, and stackup information needed to fabricate and assemble the connector evaluation board. There is also a generic bracket design to support the CEB while testing - *Intel® Generic Support Bracket Design for Connector Evaluation Board*. This bracket can be used with all Intel® connector evaluation boards. All of this collateral can be found on Intel.com: (http://www.intel.com/technology/pciexpress/devnet/resources.htm)

Connector Verification

Connector performance verification is an important step to reliable, high speed interconnects. Although it is expected that many existing PCIe connectors will meet GEN3 performance expectations, measuring the connector performance, or reviewing connector measurements provided by the supplier or a 3rd party is the best means of understanding the characteristics of any one specific PCIe connector. In the long term, Intel highly encourages suppliers and customers to standardize a path for ensuring connector compliance to PCIe GEN3 performance requirements. We hope that the PCIe GEN3 connector measurement procedure and evaluation board design will help Intel, suppliers and customers to begin the discussion. Intel will require its PCIe GEN3 connector vendors to comply with the measurement procedure, *PCIe* Gen 3 Connector High Speed Electrical Test Procedure*.